UNITED STATES PATENT APPLICATION

FOR

AUTOMATED MEMORY DESIGN SYSTEM

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AUTOMATED MEMORY DESIGN SYSTEM

FIELD OF THE INVENTION

The present invention relates to memories, and more particularly to the design of memory systems.

5 ## BACKGROUND OF THE INVENTION

The design of a memory subsystem is an essential part of an embedded system. Conventionally, the design engineer manually selects the components according to the needs of the system's embedded applications. Once the components are selected, the design engineer manually designs the memory subsystem itself. This requires significant

10 engineering time and resources.

In addition, this conventional method of memory subsystem design has several risks. First, the memory subsystem design depends on the development of custom software for the embedded system. Oftentimes, late software development leads to a compromised design of the memory subsystem. At other times, software is revised after beta shipments of the

15 system requiring an expensive redesign of the whole hardware system to revise the memory subsystem design. This leads to late time to market. Avoiding redesign compromises the functions that the revised software provides and thus is not a proper solution.

Second, compromised memory subsystems or customized memory subsystems typically lead to obsolescence problems as memory devices move to higher bit capacities,

20 different packages, and new specifications or interface standards. The average life of a memory device is usually shorter than the average life of the embedded system. In many

instances, memory manufacturers are forced to build older devices which limit capacity growth.

Third, the eventual mass production of embedded systems is hampered by the volatility of prices and availability of memory devices. Carefully selecting products that adhere to the roadmap of memory manufacturers alleviates the problem slightly but usually not satisfactorily.

Accordingly, there exists a need for an automated memory design system. The automated memory design system should reduce the engineering time and resources required to design the memory subsystem of an embedded system, provide flexibility in the memory subsystem design which addresses software development, obsolescence and market volatility problems, and should address the custom requirements of many different applications.

SUMMARY OF THE INVENTION

The present invention provides a method and system for automatically providing a memory system design. The method includes: (a) receiving memory system criteria; and (b) automatically extracting at least one memory system design based upon the memory system criteria. The present invention receives criteria which includes technical and market criteria. Based on these criteria, the present invention returns memory subsystem solutions. In the preferred embodiment, the solutions are selected from libraries of multiple memory type modules which use a single memory bus. If the solution does not exist in the libraries, a new solution is created. In this manner, the engineering time and resources required in designing the memory subsystem is reduced; a flexible memory system design is provided which

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addresses software development, obsolescence and market volatility problems; and a

memory system design is provided which addresses the custom requirements of many

different applications.

BRIEF DESCRIPTION OF THE FIGURES

Figure 1 is a block diagram illustrating a preferred embodiment of an automated

memory design system in accordance with the present invention.

Figure 2 is a block diagram illustrating a process flow of the automated memory

design system in accordance with the present invention.

Figure 3 illustrates a preferred embodiment of a memory system design library in

accordance with the present invention.

Figures 4 and 5 illustrate a preferred embodiment of the single memory bus for the

library of multiple memory type modules in accordance with the present invention.

Figure 6 is a flow chart illustrating a preferred method of extraction of solutions in

the automated memory design system in accordance with the present invention.

DETAILED DESCRIPTION

The present invention provides an automated memory design system. The following

description is presented to enable one of ordinary skill in the art to make and use the

invention and is provided in the context of a patent application and its requirements.

Various modifications to the preferred embodiment will be readily apparent to those skilled

in the art and the generic principles herein may be applied to other embodiments. Thus, the

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present invention is not intended to be limited to the embodiment shown but is to be accorded the widest scope consistent with the principles and features described herein.

To more particularly describe the features of the present invention, please refer to Figures 1 through 6 in conjunction with the discussion below.

5   Figure 1 is a block diagram illustrating a preferred embodiment of an automated memory design system in accordance with the present invention. The automated memory design system 100 accepts generalized or specific criteria from a design engineer 104 on relevant system and memory needs for an application and a description of relevant aspects of the embedded system. In the preferred embodiment, the design engineer 104 interacts with the system 100 via a user interface 102. The user interface 102 guides the design engineer 104 through the input of various criteria. The criteria can include both technical and market criteria. Technical criteria includes, but is not limited to, the memory types needed, the minimum and maximum capacities of each memory type, the data bus width of each memory type, etc. They can also include a description of the processing units, performance specifications, environmental requirements, physical constraints, etc. Market criteria includes, but is not limited to, price, availability, and upgradability of various components. Based on these criteria, the automated memory design system 100 returns one or more solutions to the design engineer 104 from which the design engineer 104 may choose.

Figure 2 is a block diagram illustrating a process flow of the automated memory design system 100 in accordance with the present invention. The preferred embodiment of the system 100 comprises the user interface 102, libraries 108 of memory system designs which use the same single memory bus 304, and a software 106 which extracts solutions and

design tools, guides, and literature from the libraries 108. First, the design engineer 104

describes the embedded system, generalizes the memory needs, and inputs these criteria into

the memory design system 100 via the user interface 102. The software 106 then processes

the criteria, via step 202. The processing includes the performance of any required

computations. It also includes the screening of the criteria received from the design engineer

104 for viability given the constraints of the embedded system, such as the specifications of

its memory controller and processing unit, or the range of available specifications of a

memory device type. Using the processed criteria, the software 106 next extracts the

solutions, via step 204. In the preferred embodiment, the solutions are extracted from the

libraries 108. If a possible solution does not exist in the libraries 108, then a new solution is

created, via step 208. A new memory subsystem may be built based upon this new solution.

Based on the extracted solutions, relevant and corresponding design tools, guides, and

information will be compiled for delivery in the proper format, via step 210, to the design

engineer 104 using the user interface 102.

Figure 3 illustrates a preferred embodiment of a memory system design library in

accordance with the present invention. Each of the libraries 108 comprises a plurality of

multiple memory type modules 302.1-302.x using the same single memory bus 304. The

multiple memory type modules 302.1-302.x in each of the libraries 108 use the single

memory bus 304 to communicate with a processor (not shown) of the embedded system. In

the preferred embodiment, each multiple memory type module 302.1-302.x can be the whole

or part of the memory subsystem for one or more embedded system applications. Each of

the multiple memory type modules 302.1-302.x varies by the combination of memory

capacities, memory subsystem architecture, and/or combinations of performance, power, and

other specifications. The software 106 selects one or more of the modules 302.1-302.x as

the memory subsystem design solutions which addresses the design engineer's criteria.

Selecting from a library of designs reduces the time and effort of designing the memory

subsystem significantly.

The libraries 108 of multiple memory type modules is further described in co-

pending US patent application entitled "Library Of Multiple Memory Type Modules Using

A Single Memory Bus", serial no. (1928P), filed on __, assigned to the assignee of the

present application. The preferred embodiment of the multiple memory-type module 302.1-

302.x is further described in co-pending US patent application entitled "Multiple Memory

Type Module Using a Single Memory Bus", serial no. (1926P), filed on ___, assigned to

the assignee of the present application. Applicant hereby incorporates these applications by

reference.

Each module 302.1-302.x can have a minimum of one or two devices per memory

type, depending on the type, and thus provides greater granularity. It provides the benefits of

memory modularity, where none was cost effective with the conventional memories, and

leads to simpler design efforts because each uses the single memory bus 304. Each module

302.1-302.x also can be expanded from its minimum configuration.

Figures 4 and 5 illustrate a preferred embodiment of the single memory bus for the

library of multiple memory type modules in accordance with the present invention. Figure 4

illustrates the architecture of the single memory bus in accordance with the present

invention. The single memory bus 60 is for communicating data and providing

programming access to the memory devices within the system memory 70. In the preferred

embodiment, the system memory 70 is the multiple type memory module in accordance with

the present invention. The single memory bus is disclosed in United States Patent No.

6,067,593, filed on July 18, 1997, issued on May 23, 2000, and assigned to the assignee of

5   the present application. Applicant hereby incorporates this patent by reference. The term

"single memory bus", as used in this specification, is used interchangeably with the term

"universal memory bus", as used in U.S. Patent No. 6,067,593.

Figure 5 illustrates the channel architecture of the single memory bus in accordance

with the present invention. The single memory bus 60 consists of a primary channel 62 for

10   communicating boot data to activate a host system and normal data thereafter, an

identification channel 64 for communicating data describing the device composition of the

system memory 70, an expansion channel 66 for providing programming and data access to

a memory device subsequently added to the system memory 70, and a programming channel

68 for providing programming access to each programmable memory device within the

15   system memory 70. The primary channel 62 is generally comprised of power, address, data,

and control lines which are necessary to establish a communication link between the central

processing unit 60 (CPU) and the system memory 70. The identification channel 64 is

generally composed of data and control lines for communicating identification data which

describes the device composition of the system memory 70 to the host CPU 50. The

20   expansion channel 66 is composed generally of additional data, address and/or programming

lines which can be selectively activated to provide address, data, or programming signals to

a subsequently added memory device. The programming channel 68 generally consists of

lines which provide programming and control signals necessary to program the serial or parallel programmable memory devices resident within the system memory. In the preferred embodiment, the programming channel consists of a dedicated sub-channel 68A which is active only during programming operations and a dual function sub-channel 68B which

5 communicates programming signals during programming operations while providing address, and or control signals during normal data transfer operations.

In this manner, the automated memory design system 100 in accordance with the present invention provides a design guide and tool to assist the design engineer 104 in developing comprehensive and riskless memory subsystem designs. The automated memory

10 design system 100 significantly reduces the memory design effort of the design engineer 104. This saves valuable engineering time and resources which may be used for other more vital and complicated areas of the end product. The automated memory design system 100 also allows the design engineer 104 to quickly redesign the memory subsystem if changes in software requirements or hardware direction occur because a new solution is simply

15 extracted from the libraries 108.

Although the present invention is described with the extraction of solutions from a library, one of ordinary skill in the art will understand that memory design solutions may be extracted from other forms of memory collections. Although the present invention is described with the library, the multiple memory type module, and the single memory bus

20 above, one of ordinary skill in the art will understand that other types of memories and buses may be used. Although the present invention is described in the context of an embedded system, one of ordinary skill in the art will understand that the present invention may be

applied to other systems with discreet components. These do not depart from the spirit and scope of the present invention.

Figure 6 is a flow chart illustrating a preferred method of extraction of solutions in the automated memory design system in accordance with the present invention. First, a library type is selected, via step 602, based upon the processed system information inputted by the design engineer 104. Example system information includes, but is not limited to, a data bus width, physical requirements, a processor, an external bus speed, and an operating temperature range. In the preferred embodiment, the selected library type has a maximum bus width, a form factor type, and a connector type which matches the system information. For illustrative purposes, assume that a library type with a 32-bit data bus, a small-outline dual in-line module (SODIMM) form factor, and a dynamic random access memory (DRAM) SODIMM connector is selected based upon the inputted criteria.

Next, a family of multiple memory type modules in the selected library type is selected, via step 604. A "family", as used in this specification, refers to a particular combination of memory device types. Multiple memory type modules with the same combination of memory device types belong in the same family. The family of multiple memory type modules is selected based upon memory choice information inputted by the design engineer 104.

Next, the first memory device type is selected for further processing, via step 606. For the illustration, assume the following memory choices were inputted: DRAM, Parallel Flash, Serial Flash, and a Serial electrically erasable programmable read-only memory (EEPROM). The DRAM is first selected for further processing, via step 606.

Next, the memory device(s) of the memory device type is selected, via step 608, based upon criteria inputted for this memory device type. For the illustration, assume that technical criteria inputted for the DRAM includes the DRAM type of synchronous DRAM (SRAM), the DRAM performance of PC100/CL3, the DRAM bus width of 32-bits, no ECC/Parity requirement, the maximum megabyte (MB) capacity of 64 MB, the minimum MB capacity of 16 MB, and the desired MB capacity of 32 MB. Inputted market criteria includes lowest cost, most available, and lowest power consumption. Based upon the technical criteria, one or more SDRAM memory devices are selected. Then, from these SDRAM devices, those which address the market criteria are selected. Thus, assume that three SDRAM devices address the technical criteria. Then, a first SDRAM device which has the lowest cost is selected; a second SDRAM device which is the most available is selected; and a third SDRAM device with the lowest power consumption is selected. The first, second, and third selected SDRAM devices may be the same or different devices.

Next, the construction of the multiple memory type module is computed, via step 610, for the memory device type. The construction refers to the number of devices and spaces for the memory device type for each criteria. For the illustration, the number of devices and spaces is computed for the first, second, and third SDRAM memory devices. Thus, a number of the first memory device and spaces are computed for the first SDRAM device which has the lowest cost; a number of the second memory device and spaces are computed for the second SDRAM which is the most available; and a number of the memory device and spaces are computed for the third SDRAM which has the lowest power consumption.

Next, the architecture of the multiple memory type module is computed, via step 612. The architecture is a function of the number of memory devices for each memory device type, the width of each memory device type's data bus, and the data bus widths for individual memory devices. The computed architecture can include the appropriate number of banks and chips selects per memory device type for each criteria. Steps 608 through 612 are repeated for each memory device type, via step 614. In the illustration, steps 608 through 612 are repeated for the Parallel Flash, the Serial Flash, and the Serial EEPROM.

Then, specific multiple memory type modules from the selected family of multiple memory type modules is determined for each market criteria, via step 616. The selected multiple memory type modules have the inputted memory device types, the computed construction, and the computed architecture. These modules are the memory system solutions which address the technical and market criteria inputted by the design engineer 104. If any of the determined multiple memory type modules does not exist in the library 108, via step 618, then a new solution, in the form of a design of the needed multiple memory type module, is created, via step 208. The solutions are then displayed to the design engineer 104 using the user interface 102, via step 210.

Although the present invention is described with the solution extraction described above, one of ordinary skill in the art will understand that other methods may be used to extract solutions without departing from the spirit and scope of the present invention.

An automated memory design system has been disclosed. The automated memory design system receives criteria from a design engineer, which includes technical and market criteria. Based on these criteria, the memory design system returns a set of memory

subsystem solutions from which the design engineer may choose. In the preferred

embodiment, the solutions are selected from libraries of multiple memory type modules

which use a single memory bus. If the solution does not exist in the libraries, a new solution

is created. In this manner, the engineering time and resources required in designing the

5   memory subsystem is reduced; a flexible memory system design is provided which addresses

software development, obsolescence and market volatility problems; and a memory system

design is provided which addresses the custom requirements of many different applications.

Although the present invention has been described in accordance with the

embodiments shown, one of ordinary skill in the art will readily recognize that there could

10   be variations to the embodiments and those variations would be within the spirit and scope

of the present invention. Accordingly, many modifications may be made by one of ordinary

skill in the art without departing from the spirit and scope of the appended claims.